UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,144	01/04/2002	Kazuo Ishimoto	81784.0247	2423

26021 7590 01/29/2007

HOGAN & HARTSON L.L.P.
1999 AVENUE OF THE STARS
SUITE 1400
LOS ANGELES, CA 90067

EXAMINER	
AGGARWAL, YOGESH K	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/041,144	ISHIMOTO ET AL.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/21/2006 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki (US Patent # 5,990,952), Egawa et al. (US Patent # 5,572,256) and further in view of Murayama et al. (US Patent # 4,686,573).

[Claim 1]

Hamasaki teaches a method for driving a solid state imaging device (figure 1) comprising accumulating information charges generated in a plurality of light receiving pixels (figure 1, sensor 1) during a first period in portions of vertical shift registers (2) corresponding to each odd

line and in portions of vertical shift registers corresponding to each even line (col. 4 lines 20-41, figure 2), vertically transferring the information charges (figure 4A, charge Q1 and Q2) accumulated in the portions of vertical shift registers (2) corresponding to each odd line to the portions of vertical shift registers corresponding to each adjacent even line, compounding the information charges (Q1 + Q2) originated from the portions of vertical shift registers corresponding to each odd line into the information charges accumulated in the portions of vertical shift registers corresponding to each adjacent even line, and holding resultant information charges in the portions of vertical shift registers corresponding to each even line (col. 4 lines 41- 67, Col. 5 lines 22-28, figures 4A, 4B and 4C),

accumulating information charges generated in a light receiving pixel in each odd line (Q1`) during a second period (figure 3 shows short exposure time) in the portions of vertical shift registers (2) corresponding to each odd line, and of accumulating information charges generated in a light receiving pixel in each even line (Q2`) during the second period in the portions of vertical shift registers corresponding to each even line in addition to the information charges that are already accumulated therein (col. 4 line 67- col. 5 line 21, col. 5 lines 29-30, figures 4A-4D); transferring the information charges accumulated in the portions of vertical shift registers corresponding to each odd line and the information charges accumulated in the portions of vertical shift registers corresponding to each even line to a horizontal shift registers (col. 6 lines 25-37).

Hamasaki teaches that the signal charges (Q1 + Q2) and (Q1` + Q2`) are moved one line at a time from the CCD vertical shift register 2 to the horizontal shift register 3 and then they are sequentially transferred in the horizontal direction but fails to teach compounding these

information charges originated from the portions of vertical shift registers corresponding to each even line into the information charges that are accumulated during the first period and are compounded in the horizontal shift register originated from the portions of vertical shift registers corresponding to each odd line into the information charges originated from the portions of vertical shift registers corresponding to each even line; and driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device.

However Egawa et al. teaches that charges transferred during the first field that are accumulated in period Tb and Ta in pixels PD1 and PD3 are added in the vertical CCD as Qa + Qb (col. 5 line 55-col. 6 line 9, figure 4).

Therefore taking the combined teachings of Hamasaki and Egawa, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to compound these information charges originated from the portions of vertical shift registers corresponding to each even line into the information charges that are accumulated during the first period in order to prevent the signal-to-noise ratio from deteriorating thereby producing a higher-quality reproduced image as taught in Egawa (col. 3 lines 12-22).

Hamasaki in view of Egawa fail to teach charges read out in the two different periods being compounded in the horizontal shift register originated from the portions of vertical shift registers corresponding to each odd line into the information charges originated from the portions of vertical shift registers corresponding to each even line; and driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device.

However Murayama et al. teaches that charges from an odd row and an even number row are added in the horizontal transfer section 116 after no charge division (by setting w to 0) and then driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device (212) in order to minimize the flicker noise associated with an interlace scanning process used together with the frame signal store system (col. 5 line 36-col. 6 line 6).

Therefore taking the combined teachings of Hamasaki, Egawa and Murayama, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have added the charges generated in the odd and even lines in the horizontal transfer section 116 after no charge division (by setting w to 0) and then driving the horizontal shift register after compounding in the horizontal shift register to obtain an information output of the solid state imaging device (212) in order to minimize the flicker noise associated with an interlace scanning process used together with the frame signal store system.

[Claim 2]

Hamasaki teaches that the duration of the second period is lesser than the first exposure period, which means lesser charges are generated during the second exposure period (col. 5 line 1).

[Claim 3]

Hamasaki also teaches that the second exposure time is a predetermined time (col. 5 line 1), therefore it would be inherent that the amount of information charges generated in a light receiving pixel corresponding to a maximum luminance portion of an object during the second period falls within a predetermined range relative to the charge storage capacity of the light receiving pixel.

[Claim 7]

Hamasaki teaches that the light receiving pixels are arranged in a matrix form (col. 3 line 60-64).

[Claim 8]

Hamasaki teaches in figures 4A and 4B that Q1 and Q2 are being independently vertically transferred from the pixels in the odd and even line.

5. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamasaki (US Patent # 5,990,952) in view of Egawa et al. (US Patent # 5,572,256)

[Claim 11]

Hamasaki teaches a method for driving a solid state imaging device (figure 1) comprising accumulating information charges generated in a plurality of light receiving pixels (figure 1, sensor 1) during a first period in portions of vertical shift registers (2) corresponding to each odd line and in portions of vertical shift registers corresponding to each even line (col. 4 lines 20-41, figure 2), vertically transferring the information charges (figure 4A, charge Q1 and Q2) accumulated in the portions of vertical shift registers (2) corresponding to each odd line to the portions of vertical shift registers corresponding to each adjacent even line, compounding the information charges (Q1 + Q2) originated from the portions of vertical shift registers corresponding to each odd line into the information charges accumulated in the portions of vertical shift registers corresponding to each adjacent even line, and holding resultant information charges in the portions of vertical shift registers corresponding to each even line (col. 4 lines 41- 67, Col. 5 lines 22-28, figures 4A, 4B and 4C),

accumulating information charges generated in a light receiving pixel in each odd line (Q1`) during a second period (figure 3 shows short exposure time) in the portions of vertical shift

registers (2) corresponding to each odd line, and of accumulating information charges generated in a light receiving pixel in each even line (Q2`) during the second period in the portions of vertical shift registers corresponding to each even line in addition to the information charges that are already accumulated therein (col. 4 line 67- col. 5 line 21, col. 5 lines 29-30, figures 4A-4D); transferring the information charges accumulated in the portions of vertical shift registers corresponding to each odd line and the information charges accumulated in the portions of vertical shift registers corresponding to each even line to a horizontal shift registers (col. 6 lines 25-37).

Hamasaki teaches that the signal charges (Q1 + Q2) and (Q1` + Q2`) are moved one line at a time from the CCD vertical shift register 2 to the horizontal shift register 3 and then they are sequentially transferred in the horizontal direction but fails to teach compounding these information charges originated from the portions of vertical shift registers corresponding to each even line into the information charges that are accumulated during the first period

However Egawa et al. teaches that charges transferred during the first field that are accumulated in period Tb and Ta in pixels PD1 and PD3 are added in the vertical CCD as Qa + Qb (col. 5 line 55-col. 6 line 9, figure 4).

Therefore taking the combined teachings of Hamasaki and Egawa, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to compound these information charges originated from the portions of vertical shift registers corresponding to each even line into the information charges that are accumulated during the first period in order to prevent the signal-to-noise ratio from deteriorating thereby producing a higher-quality reproduced image as taught in Egawa (col. 3 lines 12-22).

[Claim 12]

Hamasaki teaches that the duration of the second period is lesser than the first exposure period, which means lesser charges are generated during the second exposure period (col. 5 line 1).

[Claim 13]

Hamasaki also teaches that the second exposure time is a predetermined time (col. 5 line 1), therefore it would be inherent that the amount of information charges generated in a light receiving pixel corresponding to a maximum luminance portion of an object during the second period falls within a predetermined range relative to the charge storage capacity of the light receiving pixel.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 4-6, 9 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Egawa et al. (US Patent # 5,572,256).

[Claim 4]

Egawa teaches a method for driving a solid state imaging device comprising:

accumulating during a first period information charges generated in light receiving pixels in each odd line and of accumulating during a second period information charges generated in the light receiving pixels in each even line, the second period being shorter than the first period (e.g. charges transferred during the first field that are accumulated in period Tb and Ta in pixels

PD1 and PD3 are added in the vertical CCD as Qa + Qb col. 5 line 55-col. 6 line 9, figure 4, Tb is shorter than Ta as shown in figure 2b).

vertically transferring the information charges accumulated in the light receiving pixels (PD1) in each odd line and the information charges accumulated in the light receiving pixels in each even (PD3) line to a horizontal shift register (H-CCD, figure 1) after accumulating and compounding the information charges originating from the light receiving pixels in each odd line with the information charges originating from the light receiving pixels in each even line (See col. 5 line 55-col. 6 line 9, figure 4 charges form PD1 (Qb) and PD3 (Qb) are accumulated and compounded as Qa + Qb) ; and

driving the horizontal shift register after compounding to obtain an information output of the solid state imaging device (col. 6 lines 6-9).

[Claim 5]

Egawa teaches (figure 2b) that the duration of the second period (Tb) is lesser than the first exposure period (Ta), which means lesser charges are generated during the second exposure period.

[Claim 6]

Egawa also teaches that the second exposure time Tb is controlled by the driving pulse B generator and therefore is a predetermined time (col. 8 lines 47-57), therefore it would be inherent that the amount of information charges generated in a light receiving pixel corresponding to a maximum luminance portion of an object during the second period falls within a predetermined range relative to the charge storage capacity of the light receiving pixel.

[Claim 9]

Egawa teaches that the light receiving pixels are arranged in a matrix form (See figure 1).

[Claim 10]

Egawa teaches in figures 4A and 4B that Qa and Qb are being independently vertically transferred from the pixels in the odd and even line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivek Srivastava can be reached on (571)-272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YKA
January 22, 2007

VIVEK SRIVASTAVA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600